TECHNISCHE UNIVERSITÄT DRESDEN

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Chair of Highly-Parallel VLSI Systems and Neuro-Microelectronics

LAB REPORT NEUROMORPHIC VLSI SYSTEMS

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CONTENTS

1 INTRODUCTION

This report details the design, simulation and layout of an integrated operational transamplifier (OTA). The first chapter describes the steps taken in approximating EKV model transistor parameters for the NMOS and PMOS transistors used in the design. These are then utilized in the third chapter where theoretical considerations serve as a starting point for the dimensioning of the circuit's transistors. Through simulation these dimensions are then optimized so that the circuit meets it's required specifications. Finally, a circuit layout is created, checked for correctness and used to create a parasitic model of the circuit which is again simulated, whereby simulation results are compared with those obtained from the schematic.

2 PARAMETER EXTRACTION

Note: this material was covered in the exercises and is only included for the sake of completeness.

2.1 NMOS

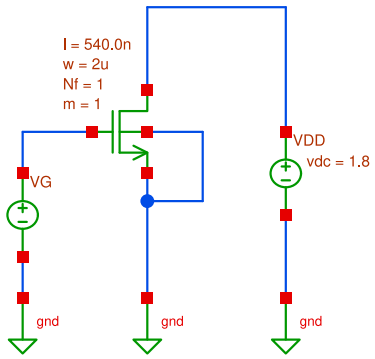


Figure 2.1: Circuit used for NMOS parameter extraction

2.1.1 DETERMINING *n*

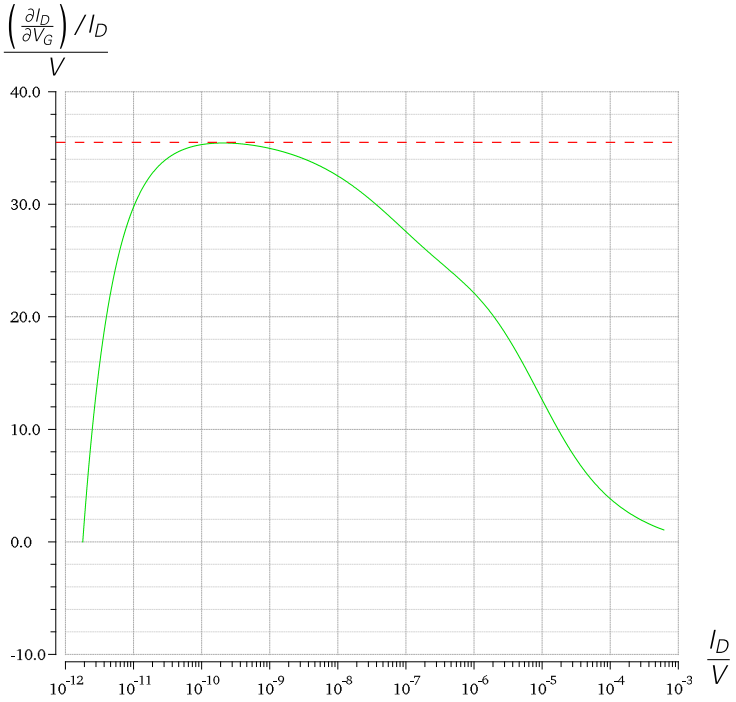


Figure 2.2: $\left(\frac{\partial I_D}{\partial V_G}\right)/I_D$ as a function of I_D

Figure 2.2 shows $\left(\partial I_D/\partial V_G\right)/I_D$ as a function of I_D, obtained by simulation of the circuit in Figure 2.1. For a transistor in weak inversion as well as saturation, $\left(\partial I_D/\partial V_G\right)/I_D$ should be approximately equal to $(nU_T)^{-1}$, where $U_T = kT/q$ (with $T = 27°C/300.15K$). From this, we can estimate n by reading off the curve's absolute value around it's minimum, which in this case is approximately $35.5V^{-1}$, and then calculating:

$$n \approx \frac{q}{35.5V^{-1} \cdot kT} \approx 1.09 \tag{2.1}$$

2.1.2 DETERMINING $\mu C''_{ox}$ AND V_{T0}

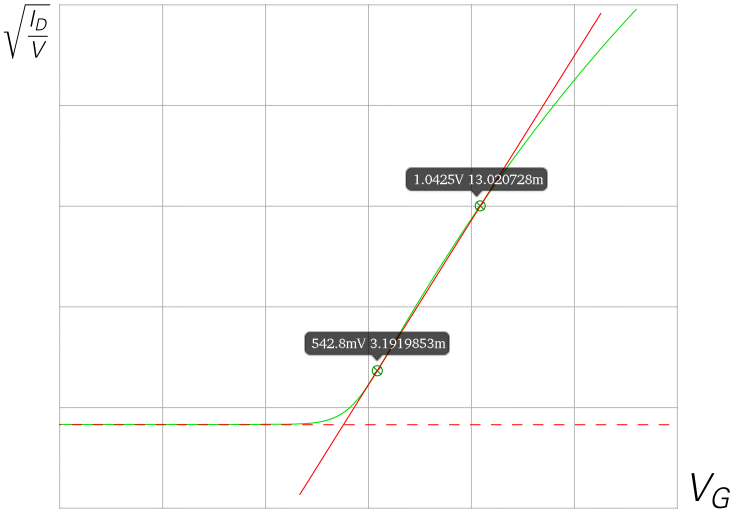


Figure 2.3: $\sqrt{I_D}$ as a function of V_G

Figure 2.3 shows $\sqrt{I_D}$ as a function of V_G, again obtained through simulation of the circuit in Figure 2.1. A straight line approximation of the curve is shown in red. From the two points $(V_{G,1}, \left(\sqrt{I_D}\right)_1)$ and $(V_{G,2}, \left(\sqrt{I_D}\right)_2)$ defining this line approximation, we can obtain both it's slope m and it's value b at $V_G = 0$ since:

$$mV_{G,1} + b = \left(\sqrt{I_D}\right)_1$$
$$mV_{G,2} + b = \left(\sqrt{I_D}\right)_2$$

Solving these equations for m and b we obtain:

$$m = \frac{\left(\sqrt{I_D}\right)_2 - \left(\sqrt{I_D}\right)_1}{V_{G,2} - V_{G,1}}$$

$$b = \frac{\left(\sqrt{I_D}\right)_1 V_{G,2} - \left(\sqrt{I_D}\right)_2 V_{G,1}}{V_{G,2} - V_{G,1}}$$

Since according to the EKV model $\sqrt{I_D} = \sqrt{\frac{\beta}{2n}}(V_G - V_{T0})$, it holds that $m = \sqrt{\frac{\beta}{2n}}$ and $b = -mV_{T0}$. Solving for β and V_{T0} we obtain:

$$\beta \approx 2n \left(\frac{\left(\sqrt{I_D}\right)_2 - \left(\sqrt{I_D}\right)_1}{V_{G,2} - V_{G,1}} \right)^2$$

$$V_{T0} \approx \frac{\left(\sqrt{I_D}\right)_2 V_{G,1} - \left(\sqrt{I_D}\right)_1 V_{G,2}}{\left(\sqrt{I_D}\right)_2 - \left(\sqrt{I_D}\right)_1}$$

Resulting in:

$$\beta \approx 0.85 \frac{mA}{V^2} \Rightarrow \mu C''_{ox} = \left(\frac{W}{L}\right)^{-1} \cdot \beta \approx 229.5 \frac{\mu A}{V^2} \tag{2.2}$$

$$V_{T0} \approx 0.38V \tag{2.3}$$

2.2 PMOS

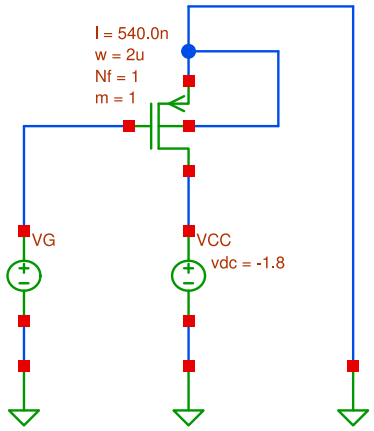


Figure 2.4: Circuit used for PMOS parameter extraction

Performing similar steps for the circuit in Figure 2.4, we can determine n, $\mu C''_{ox}$ and V_{T0} for the respective PMOS. Figure 2.5 and 2.6 show the relevant simulation results. Overall we obtain:

$$n_n \approx 1.09 \tag{2.4}$$

$$\left(\mu C''_{ox}\right)_n \approx 229.5 \frac{\mu A}{V^2} \tag{2.5}$$

$$V_{T0,n} \approx 0.38V \tag{2.6}$$

and:

$$n_p \approx 1.43 \tag{2.7}$$

$$\left(\mu C''_{ox}\right)_p \approx 68 \frac{\mu A}{V^2} \tag{2.8}$$

$$V_{T0,p} \approx -0.47V \tag{2.9}$$

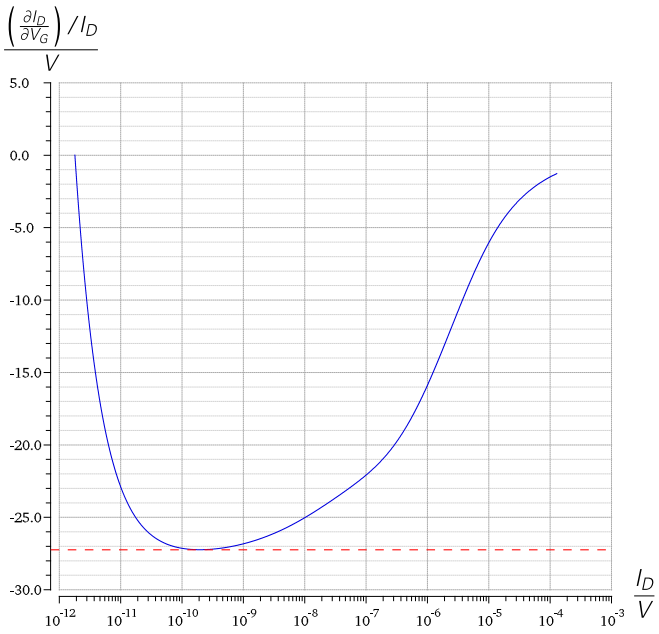


Figure 2.5: $\left(\frac{\partial I_D}{\partial V_G}\right)/I_D$ as a function of I_D

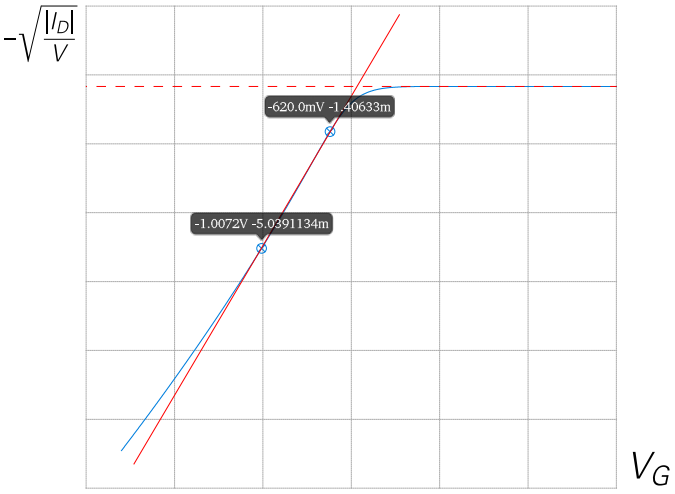


Figure 2.6: $-\sqrt{|I_D|}$ as a function of V_G

3 CIRCUIT ARCHITECTURE

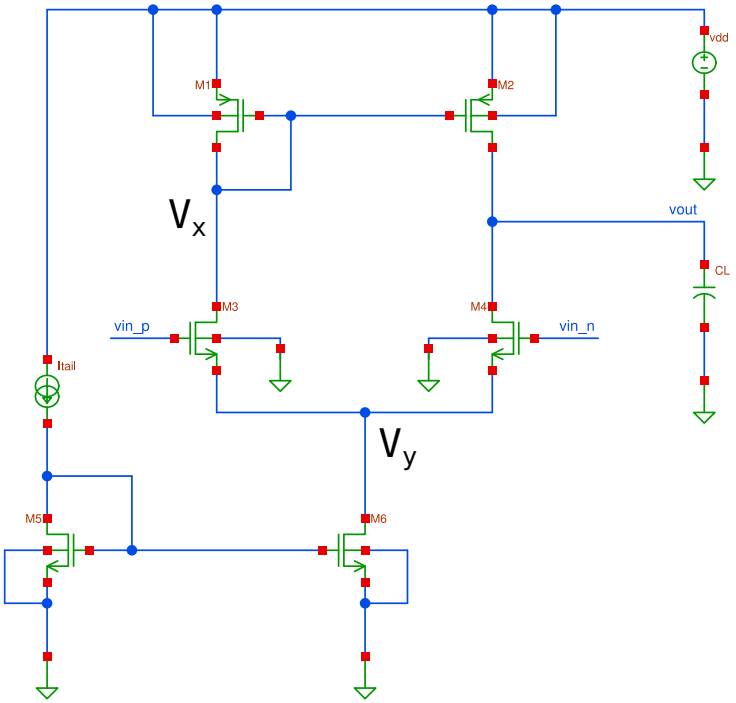


Figure 3.1: OTA circuit architecture

Figure 3.1 shows the basic single stage circuit architecture used to realize the OTA. The labels V_x and V_y denote the node voltages at those points in the cicuit which we are going to refer to later. In the following chapter we will determine rough bounds on the dimensions of transistors M1 - M6 by utilizing both the component parameters approximated in the last chapter as well as the limits and typical values given in the circuit specifications in Table 3.1.

Parameter	min	typ	max	Unit
A_V	42			dB
GBW	100			MHz
f_1	1000			kHz
$VCMo$		1.0		V
$CMRi$	0.6		1.4	V
C_L		0.5		pF
V_{DD}		1.8		V

Table 3.1: Circuit Specifications

4 DIMENSIONING

In the following sections we will use the limits given in Table 3.1 in order to determine approximate values for/bounds on the width to length ratios of transistors M1 - M6 (sometimes depending on the hitherto unknown tail current). We will also utilize the fact that due to the circuit's symmetry, the transistors forming the transistor pairs M1 and M2, M3 and M4 as well as M5 and M6 should have the same dimensions respectively.

4.1 THEORETICAL CONSIDERATIONS

4.1.1 ESTIMATING $\frac{W_1}{L_1}/\frac{W_1}{L_1}$

First, we'll use the given output common mode voltage $VCMo$ to estimate an appropriate width to length ratio for transistors M1 and M2. For a common mode signal at the circuit's inputs, half the tail current will be flowing through the left as well as the right branch of the differential amplifier. Also, the voltage V_X will be equal to the voltage V_{out} at the circuit's output which should be equal to VCMo as given in Table 3.1 in the circuit's operating range.

First of all we can observe that in order for M3 and M4 to remain in saturation for a common mode input voltage $VCMi_{max}$ at the upper end of the range given by $CMRi$, V_X/V_{out} should remain greater than $VCMi_{max} - V_{TO,n}$. Since $V_X = V_{out} = VCMo = 1.0V$ and $VCMi_{max} - V_{TO,n} \approx 1.4V - 0.38V = 1.02V$, it might be necessary to choose $VCMo$ to be slightly higher than the value given in the circuit specifications.

Now, looking at M1/M2, their source voltages are V_{DD} and their gate voltage are again $V_X = V_{out} = VCMo$. If we assume that both transistors operate in saturation, it follows for their source currents that:

$$\frac{I_{tail}}{2} = \frac{\beta_{1/2}}{2n_p}(V_{DD} - VCMo - |V_{T0,p}|)^2 \tag{4.1}$$

By solving for $\beta_{1/2}$ and then substituting $\beta_{1/2} = \left(\mu C''_{ox}\right)_p (W/L)_{1/2}$ and solving for $(W/L)_{1/2}$ we obtain:

$$\beta_{1/2} = \frac{n_p \cdot I_{tail}}{(V_{DD} - VCMo - |V_{T0,p}|)^2} \Rightarrow \left(\frac{W}{L}\right)_{1/2} = \frac{1}{\left(\mu C''_{ox}\right)_p} \cdot \frac{n_p \cdot I_{tail}}{(V_{DD} - VCMo - |V_{T0,p}|)^2} \tag{4.2}$$

By calculating this expression we find that:

$$\left(\frac{W}{L}\right)_{1/2} \approx 0.2 \cdot \left(\frac{I_{tail}}{\mu A}\right) \tag{4.3}$$

But we have to note that this is not a very reliable estimate since the result depends strongly on the values of $V_{T0,p}$ and n_p. Still, we can use this value as a starting point and then tune it until we reach the desired $VCMo$. To do this, we can solve Equation 4.1 for $VCMo$ to gain a

feeling for how strongly changes in $(W/L)_{1/2}$ are going to influence $VCMo$:

$$VCMo = V_{DD} - |V_{T0,p}| - \sqrt{\frac{n_p \cdot I_{tail}}{\beta_{1/2}}} \tag{4.4}$$

So we can see that increasing $(W/L)_{1/2}$ should lead to an increase (albeit not a proportional one) in $VCMo$.

4.1.2 ESTIMATING $\frac{W_3}{L_3}/\frac{W_4}{L_4}$

Next, we'll establish an approximate lower bound on the width to length ratio of transistors M3 and M4 from the lower bound on the circuit's gain bandwidth product. The complex gain of the circuit can (without derivation) be described by the expression:

$$\frac{\underline{V}_{out}}{\underline{V}_{in}} = -\frac{gm_4 \cdot \left(r_{DS,2} \| r_{DS,4}\right)}{1 + j\omega \left(r_{DS,2} \| r_{DS,4}\right) C_L} \tag{4.5}$$

From this we can determine an expression for the DC-Gain A_V, by setting ω to zero, as well as the pole frequency f_1, as $1/(2\pi)$ times the angular frequency at which the complex gain's absolute value reaches $1/\sqrt{2} \cdot A_V$.

$$A_V = gm_4 \cdot \left(r_{DS,2} \| r_{DS,4}\right) \tag{4.6}$$

$$f_1 = \frac{1}{2\pi \left(r_{DS,2} \| r_{DS,4}\right) C_L} \tag{4.7}$$

From this it follows for the gain bandwidth product GBW:

$$GBW = A_V \cdot f_1 = \frac{gm_4}{2\pi C_L} > GBW_{min} \tag{4.8}$$

Since transistor M4 should be in saturation, with it's drain current equal to $I_{tail}/2$, it is:

$$gm_4 = \sqrt{\frac{\beta_4 \cdot I_{tail}}{n_n}} \tag{4.9}$$

We can substitute this into Equation 4.8 and then solve for β_4 and subsequently obtain a lower bound on $(W/L)_4$ (and thus $(W/L)_3$ as well):

$$\begin{aligned} \beta_4 &= \frac{n_n \cdot gm_4^2}{I_{tail}} > \frac{4\pi^2 n_n C_L^2 GBW_{min}^2}{I_{tail}} \\ \Rightarrow \left(\frac{W}{L}\right)_{3/4} &> \frac{1}{\left(\mu C''_{ox}\right)_n} \cdot \frac{4\pi^2 n_n C_L^2 GBW_{min}^2}{I_{tail}} \approx 430 \left(\frac{I_{tail}}{\mu A}\right)^{-1} \end{aligned} \tag{4.10}$$

We can also note that since $r_{DS,2/4} \approx 2/(\lambda_{2/4} \cdot I_{tail})$ it follows from Equation 4.6 that:

$$A_V \propto \sqrt{\frac{\beta_4}{I_{tail}}} \cdot \frac{1}{\lambda_2 + \lambda_4} \tag{4.11}$$

So we should be able to increase the DC gain by increasing $(W/L)_{3/4}$ or by increasing the channel lengths of transistors M2 and M4 (since because $\lambda \propto \Delta L/L$, λ is smaller for longer channels). At the same, it follows from Equation 4.7 that:

$$f_1 \propto \lambda_1 + \lambda_2 \tag{4.12}$$

Such that increasing the channel lengths of transistors M2 and M4 is going to reduce f_1, so that we have to settle for a trade-off here.

4.1.3 ESTIMATING $\frac{W_4}{L_4}/\frac{W_5}{L_5}$

Finally, we'll derive a lower bound on the width to length ratios of transistors M5 and M6 (depending on $(W/L)_{3/4}$) from the minimum common mode input voltage $VCMi_{min} = 0.6V$. When the input reaches this minimum voltage, the voltage V_Y must remain high enough to keep M6 in saturation. Since we know that for common mode input the drain current through M3/M4 is $I_{tail}/2$, we can determine the minimum value of V_Y as $VCMi_{min}$ minus the corresponding gate source voltage drop across M3/M4 which can be obtained by solving M3/M4's drain current equation (assuming M3/M4 are in saturation):

$$\begin{aligned} \frac{I_{tail}}{2} = \frac{\beta_{3/4}}{2n_n}(V_{GS,3/4} - V_{T0,n})^2 \Rightarrow V_{GS,3/4} = \sqrt{\frac{n_n \cdot I_{tail}}{\beta_{3/4}}} + V_{T0,n} \\ \Rightarrow V_{Y,min} = VCMi_{min} - \left(\sqrt{\frac{n_n \cdot I_{tail}}{\beta_{3/4}}} + V_{T0,n}\right) \end{aligned} \tag{4.13}$$

For M6 to remain in saturation at this voltage, it should still be greater than $V_{GS,6} - V_{T0,n}$. We know that the drain current through M6 is I_{tail} and from this we can determine $V_{GS,6}$ just like we did for M3 above. It follows that:

$$\cdots \Rightarrow V_{GS,6} = \sqrt{\frac{2n_n \cdot I_{tail}}{\beta_6}} + V_{T0,n} \tag{4.14}$$

From this we can derive a lower bound on $(W/L)_6$ depending on I_{tail} and $(W/L)_{3/4}$:

$$V_{Y,min} > V_{GS,6} - V_{T0,n} \Rightarrow VCMi_{min} - \left(\sqrt{\frac{n_n \cdot I_{tail}}{\beta_{3/4}}} + V_{T0,n}\right) > \sqrt{\frac{2n_n \cdot I_{tail}}{\beta_6}} \tag{4.15}$$

$$\Rightarrow \cdots \Rightarrow \left(\frac{W}{L}\right)_6 > \frac{2}{\left((VCMi_{min} - V_{T0,n})\sqrt{\frac{(\mu C''_{ox})_n}{n_n \cdot I_{tail}}} - \left(\frac{W}{L}\right)_{3/4}^{-\frac{1}{2}}\right)^2} \approx \frac{2}{\left(3.2\left(\frac{I_{tail}}{\mu A}\right)^{-\frac{1}{2}} - \left(\frac{W}{L}\right)_{3/4}^{-\frac{1}{2}}\right)^2} \tag{4.16}$$

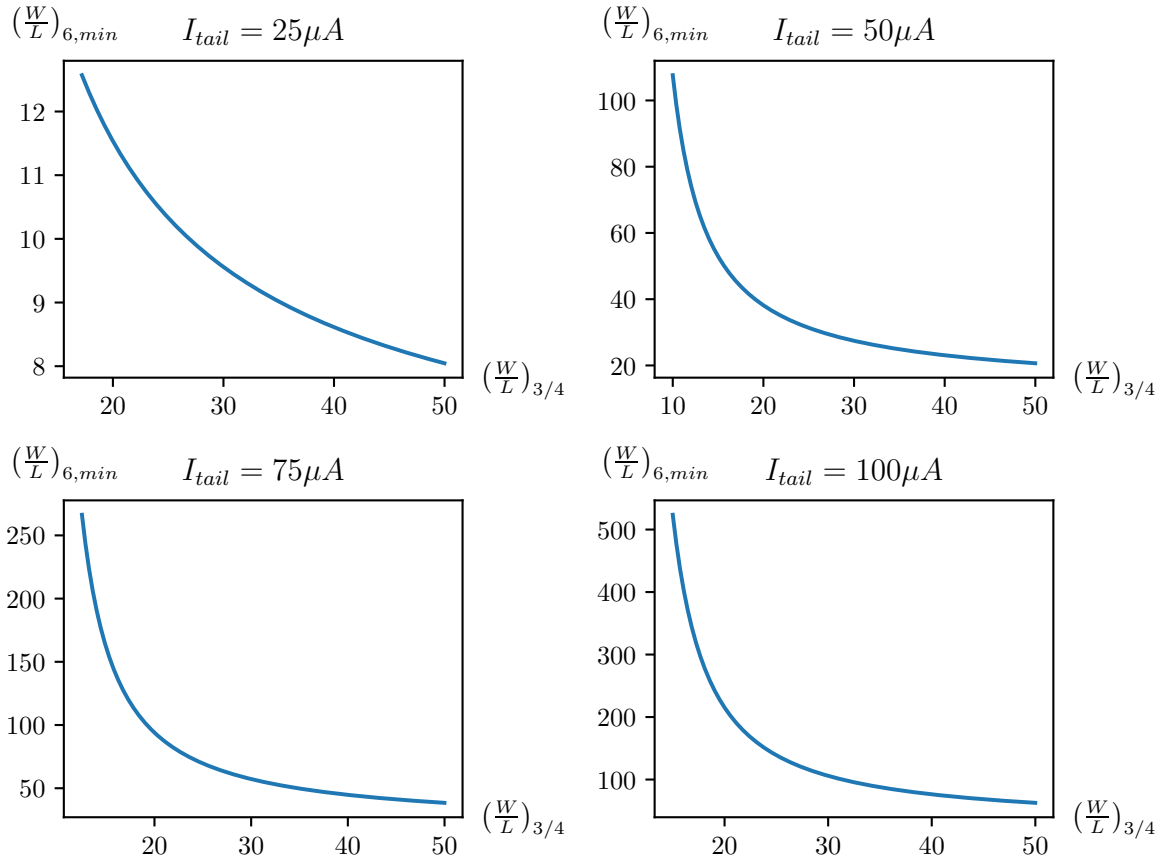


Figure 4.1: $(W/L)_{6,min}$ as a function of $(W/L)_{3/4}$ for different tail currents

Figure 4.1 shows plots of this lower bound as a function of $(W/L)_{3/4}$ for different tail currents. We can infer from this, that for all tail currents, a larger $(W/L)_{3/4}$ ratio leaves more design room for $(W/L)_6$. We can also see that for large tail currents, $(W/L)_{3/4}$ would have to be very large in order for values of $(W/L)_6$ above the corresponding lower bound to be actually realizable. This makes tail currents significantly larger than about $50\mu A$ unrealistic.

5 SIMULATION

5.1 GENERAL PROCEDURE

The theoretical results obtained so far can only provide a rough estimate. But we can still use them as a starting point and utilize the intuition obtained via the theoretical considerations to then find the right transistor dimensions, with which the circuit conforms to the specifications in Table 3.1, via experimental simulation.

Overall, our goal in parametrizing the circuit will be to minimize the resulting circuit area. We will therefore start by choosing some tail current that is compatible with the results in Figure 4.1. To find the final ratios $(W/L)_{1/2}$ and $(W/L)_{3/4}$, we will then start with very small transistors with the same channel length $L = 1\mu m$ which is sufficiently larger than the minimum channel length dictated by the technology used[1].

We will then choose the channel width of transistors M1 and M2 according to Equation 4.3 and adjust this until the desired output common mode voltage is reached. We will similarly set the channel widths of transistors M3 and M4 according to Equation 4.10 and adjust this until the gain bandwidth product is above the required minimum.

Afterwards, if the desired DC gain is not yet reached for the lower voltages in the input common mode range, we can scale up transistors M1/M2, leaving their width to length ratios untouched, until the desired gain is reached. If this does not suffice, we can also scale up M3/M4 which should also increase gain. But this is not as sensible, since as we know we can not make the channels of both M1/M2 and M3/M4 arbitrarily long because this will limit the circuit's bandwidth. So we will most likely have to limit the channel length on at least one of these pairs and doing so for M3/M4 will have the added effect of leaving more room for a larger ratio $(W/L)_{3/4}$ which will have a positive effect on the gain bandwidth product, the lower bound on $(W/L)_6$ as well as (to a lesser extent) the DC gain as well.

While doing this, we have to make sure, that M6 remains in saturation for low input common mode voltages and choose $(W/L)_6$ and $(W/L)_5$ accordingly[2].

We will repeat this procedure for several tail currents somewhere around $50\mu A$ to find out for which of these we can produce the best simulation results. A smaller tail current would in this case also reduce the circuit's static power consumption.

[1] We will not go lower than this to avoid unpredictable transistor behaviour.

[2] We could choose the dimensions of M5 to be different from those of M6 here so that the tail current is not mirrored 1:1 but we will avoid this to make the dimensioning process easier and the final layout more regular.

5.2 RESULTS

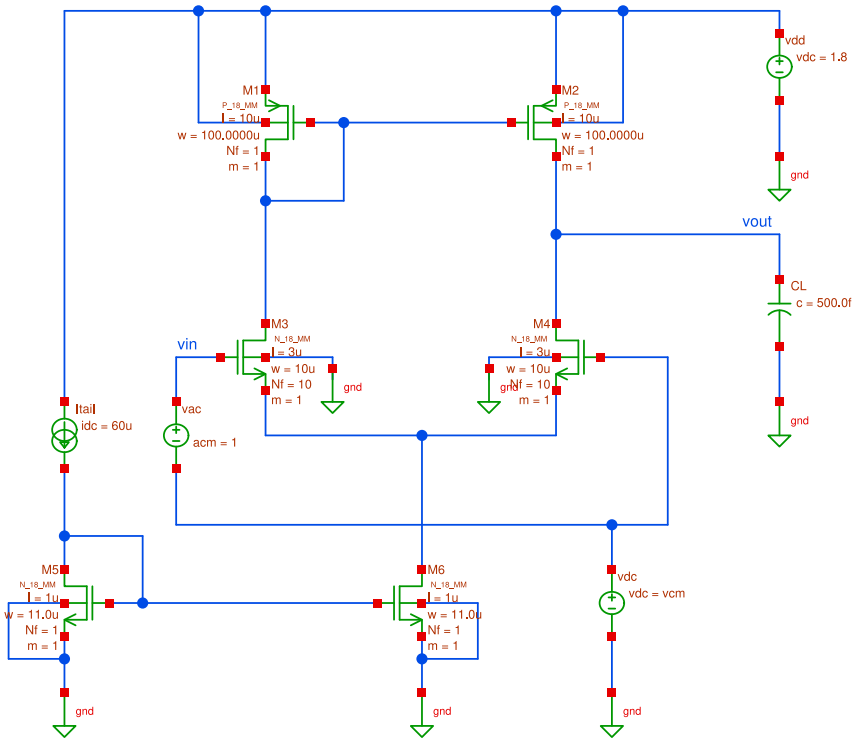


Figure 5.1: OTA testbench circuit

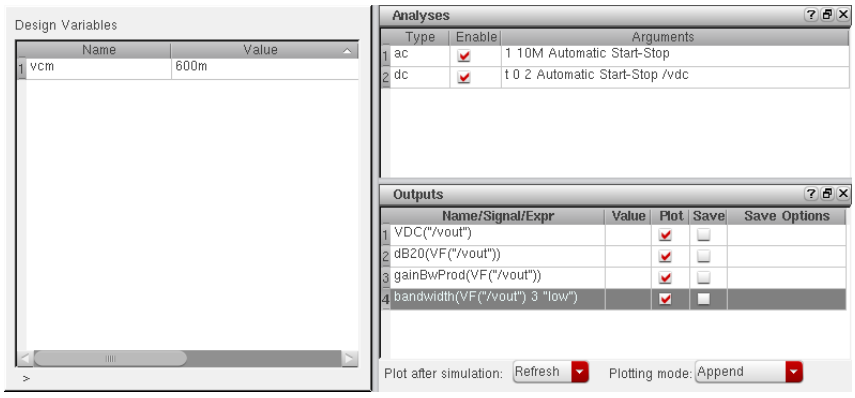


Figure 5.2: ADE simulation settings

Type	Enable	Arguments
ac	☑	0 2 Automatic Start-Stop 10 /vdc

Figure 5.3: ADE simulation settings (DC gain)

Variable	Value	Sweep?	Range Type	From	To	Step Mode	Total Steps	Inclusion List	Exclusion List
vcm	600m	☑	From/To	600m	1.4	Auto	20	1	

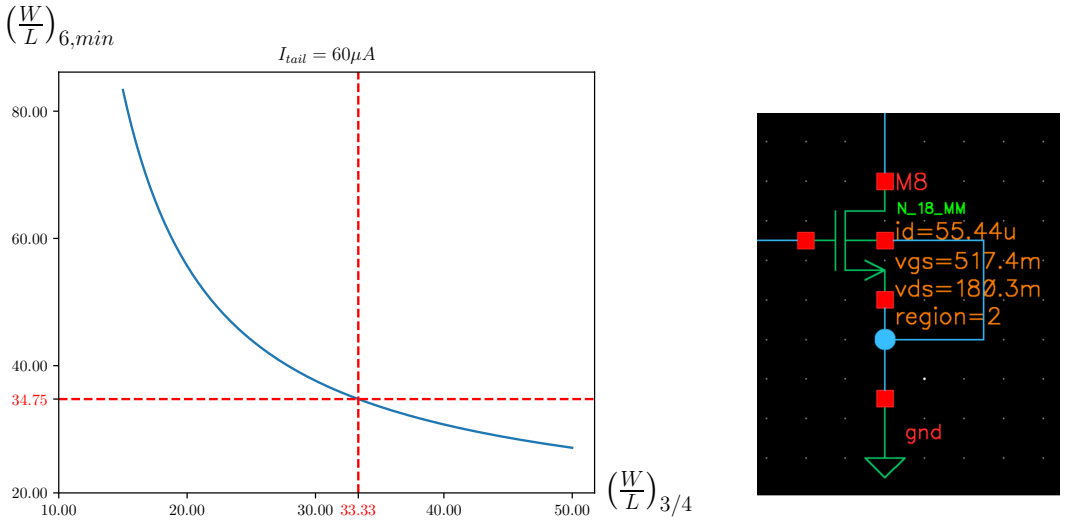
Figure 5.4: ADE parameterization

Figure 5.1 shows the test circuit setup used for the schematic simulation (for the sake of brevity already with the final transistor dimensions which were obtained through the methods de-

scribed in the last chapter and the simulation steps described below) and Figures 5.2, 5.3 and 5.4 give an overview of the simulation settings used.

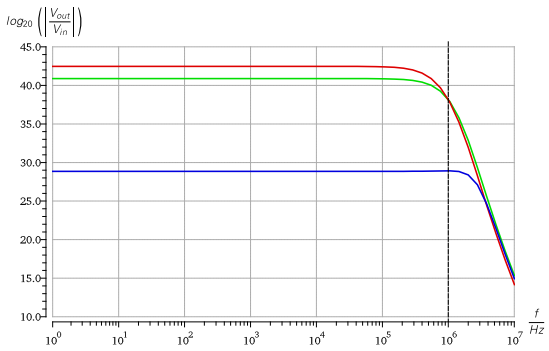
DC analysis was performed to check whether the output voltage is approximately equal to *VCMo* over the input common mode range and whether all transistors operate in saturation mode at the low and high end of the input common mode range (see Figure 5.5). AC analysis was used to plot gain (in decibels) for frequencies ranging from 1Hz to 10MHz and to calculate the associated bandwidth as well as the gain bandwidth product. Input common mode voltage was initially fixed at the lower end (600mV) here. Parametric analysis was then performed to obtain gain curves for multiple representative input common mode voltages (600mV, 1V and 1.4V) and to obtain bandwidth and gain bandwidth as a function of input common mode voltage (see Figure 5.4).

In a separate step, AC analysis was used to simulate gain at a low "almost DC" frequency of 10Hz over the whole common mode input range (see Figure 5.3).

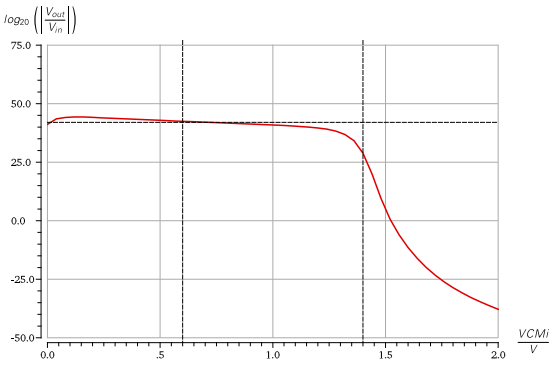


(a) (b)

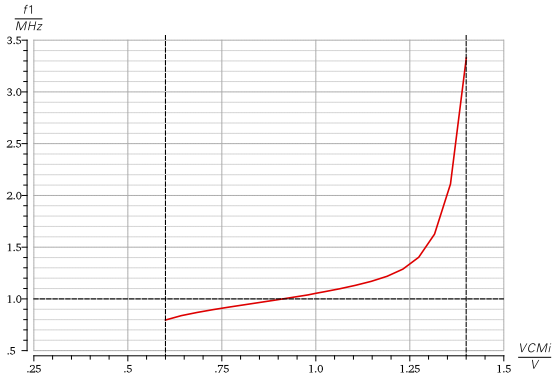
Figure 5.5: To find a suitable width to length ratio for M6 (and thus M5), starting from the theoretical minimum (5.5a), the ratio was lowered as far as possible without having M6 leave the saturation region for the minimum common mode input voltage (this can be checked by observing the *region* operating point value (5.5b)). Similarly, we can check this parameter for all the transistors at both ends of the input common mode range. The final minimal ratio for M6 ended up being a lot lower than the "theoretical" minimum (11 vs. $\approx$ 35).



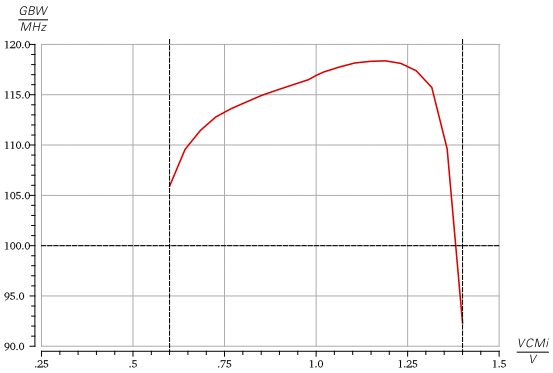
(a) Gain as a function of frequency



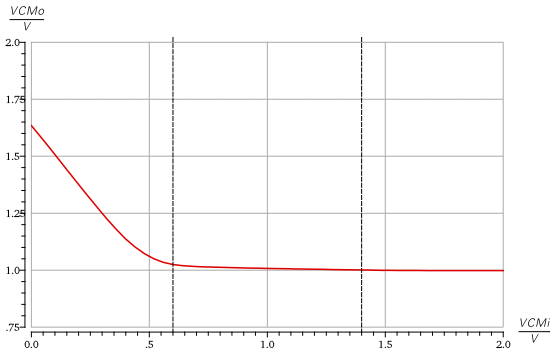
(b) Gain at 10Hz as a function of input common mode voltage



(c) bandwidth as a function of input common mode voltage



(d) gain bandwidth product as a function of input common mode voltage



(e) DC output voltage as a function of input common mode voltage

Figure 5.6: Schematic simulation results

Figure 5.6 shows the final simulation results with the transistors dimensioned as shown in Figure 5.1 and a tail current of 60µA for which the best results could be achieved. In the end very large transistors (up to 100µm in channel width) were needed for the circuit to meet the required specifications and even then, some limits could not be met over the entire input common mode range.

Figure 5.6a shows the magnitude of the AC gain for frequencies up to 10MHz for three representative common mode input voltages (600mV, 1V and 1.4V). We can see that for $VMCi$ = 600mV the DC gain is higher than the required 42dB but in the middle of the common mode input range the gain is already about 1dB below this limit. For even higher $VCMi$ the gain inevitably collapses. Much better results were not achievable with the given circuit architecture. Figure 5.6b makes this even more clear (the slightly pronounced black bars are the limits of the input common mode range and the lower DC gain limit).

Figure 5.6c and 5.6d show bandwidth and gain bandwidth product over the common mode

input range (with limits again indicated by black lines). We can see that the bandwidth falls slightly below it's lower limit for small common mode input voltages and that the gain bandwidth product stays well above it's lower limit until the just before the end of the common mode input voltage range.

Figure 5.6e shows a DC output voltage over the common mode input range which is very close to the required $VCMo$ = 1V.

Overall these results are satisfactory since each specification is only slightly (if at all) violated for limited parts of the input common mode range. If significantly better results are desired, a different circuit architecture (e.g. a two stage OTA) might be desirable.

6 CIRCUIT LAYOUT

Since the simulation results proved satisfactory, the schematic is now used as a template for the layout of the circuit. In order to compare the final layout with the schematic in Figure 3.1 that we have worked with so far, pins were added to the schematic (see Figure 6.1) and an appropriate symbol view was created (as can be seen in Figure 6.2). The transistor in Figure 6.1 are also already annotated with the fingers each transistor will be made up of in the layout.

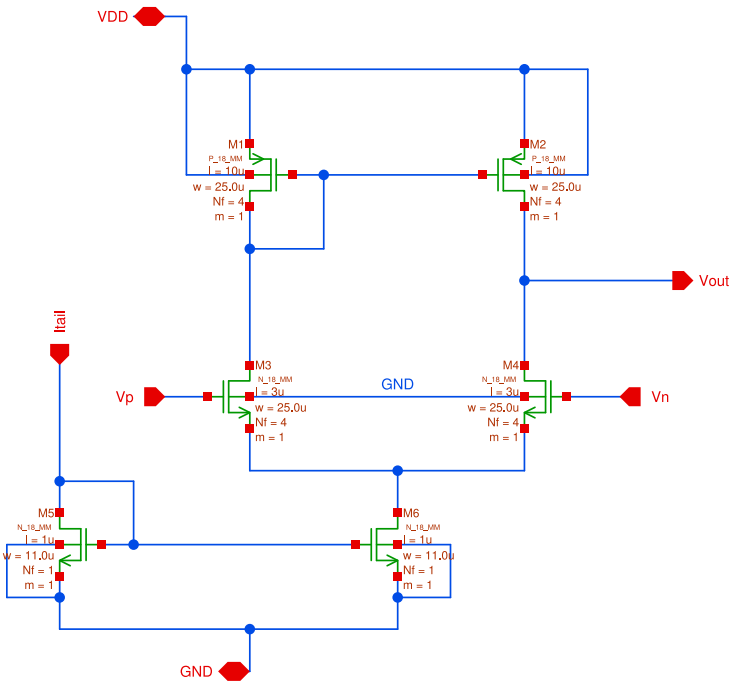


Figure 6.1: OTA circuit architecture with added pins

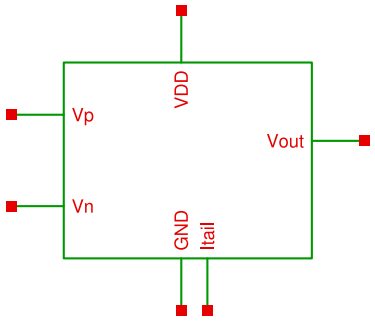


Figure 6.2: OTA symbol

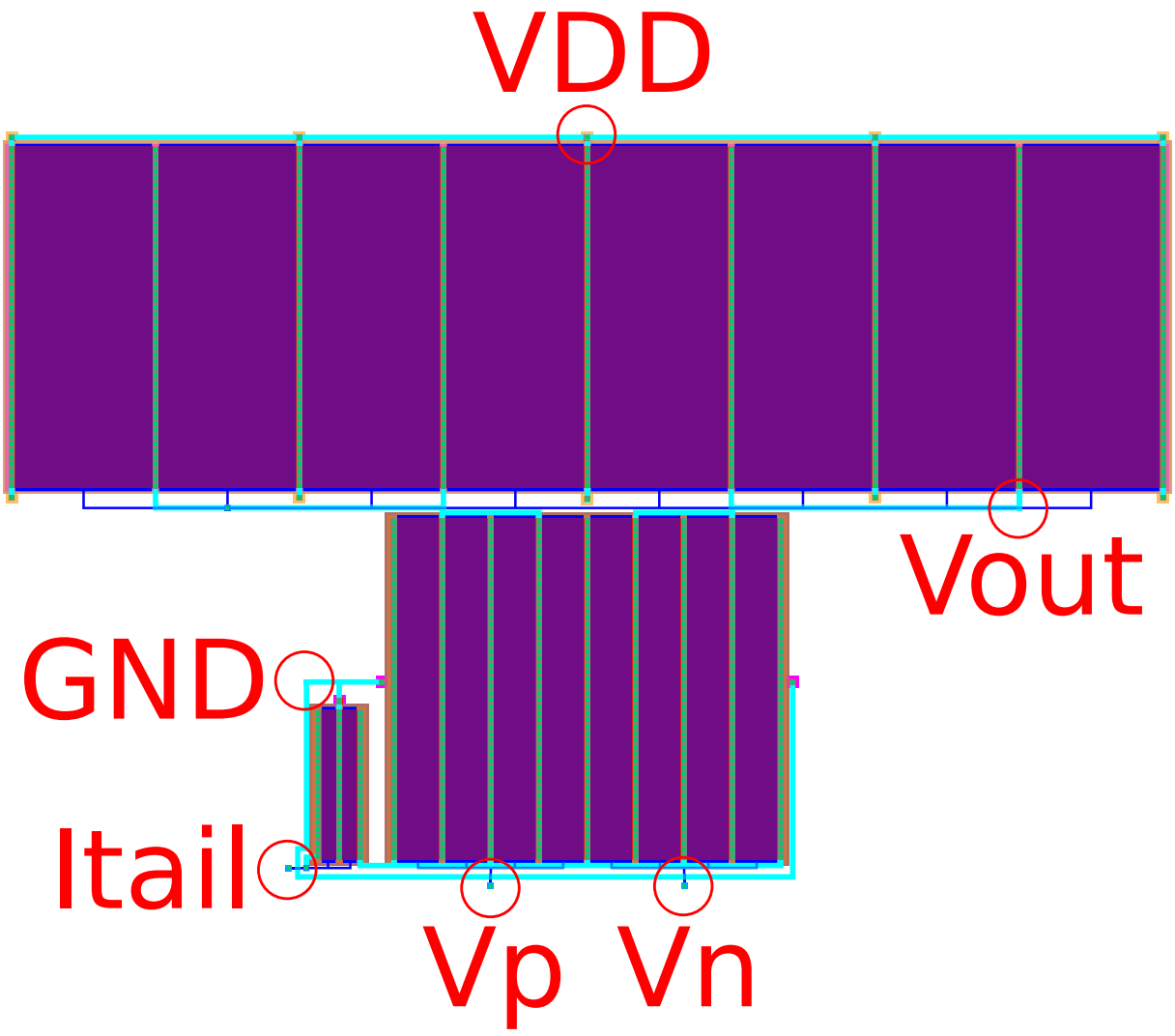


Figure 6.3: OTA layout

Figure 6.3 shows the final layout created with *Virtuoso Layout Suite L*[1]. It should be obvious that the topmost of the three "transistor blocks" realizes the two topmost PMOS in Figure 6.1, with each transistor split into four fingers. While splitting large transistors into fingers can have benefits with regard to the circuit's behaviour, here it is mainly used to allow for more "agreeable" layout dimensions. The fact that both transistors are realized in a single "block" saves a little space and should also improve transistor matching, similarly for the transistor blocks realizing the differential amplifier's two NMOS and the two NMOS forming the current mirror.

Because of the very large transistors used in the design, the connections between them contribute very little to the overall area of the layout. Nevertheless, mostly as a learning exercise, the connections are for the most part laid out with close to minimal spacing (as specified by the design rules) between each other and the transistors. Figure 6.4 exemplifies this by showing a closeup of the area around the tail current input pin. Here, the `GND` wire, which must contact the PMOS block's bulk on it's other side is laid out as close as possible around the via connecting the two NMOS's gates to the left one's drain.

[1] Note that the colour-scheme differs from that used in the editor because the image was created with the "`ICPRO → export EPS`" command, which produces an overall more "tidy" visualisation.

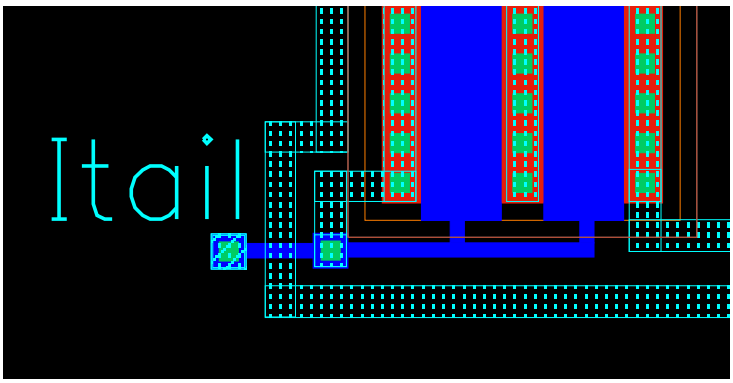
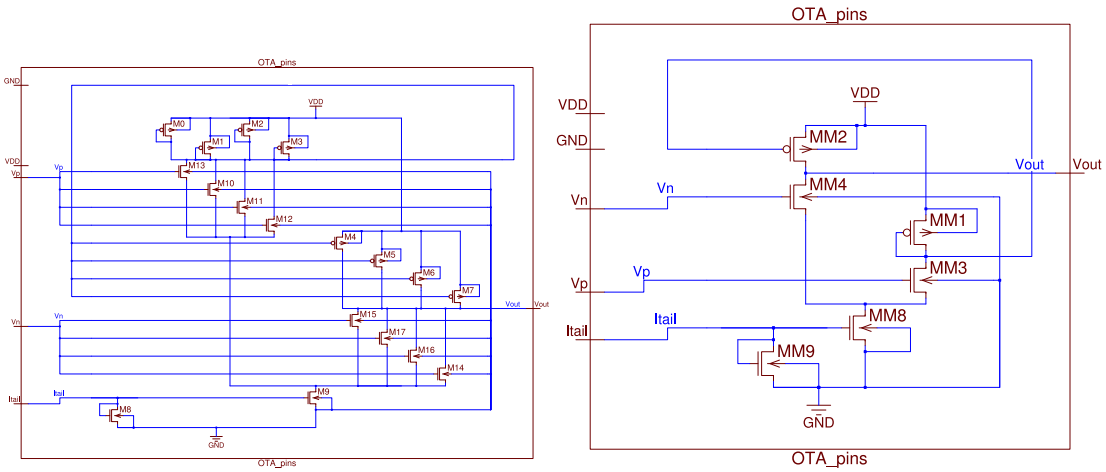


Figure 6.4: OTA layout detail

Calibre nmDRC was used to make sure that no design rules are violated by the layout and *Calibre nmLVS* was used to verify that the layout matches the original schematic. Figure 6.5 shows the circuit schematic extrapolated from the layout by nmLVS and the corresponding original schematic side by side. Because in the layout, the transistors making up the differential amplifier are split into four fingers each, each of these transistor in Figure 6.5b corresponds with four parallel (a quarter as wide) transistors in Figure 6.5a.



(a) Schematic extrapolated from layout

(b) Original schematic

Figure 6.5: Comparison of schematic extrapolated by LVS with original schematic (unimportant net names were removed from the schematics)

7 PARASITICS SIMULATION

Finally, *Calibre PEX* was used to model the parasitic effects resulting from the circuit layout. The *calibre* cellview created by PEX was simulated using the same steps as before by including it in ADE's Environments *Switch View List* (`Setup` → `Environments` → `...`) before "schematic" (see Figure 7.1) and then running the same simulations as in Figure 5.2 using the testbench circuit shown in Figure 7.2.

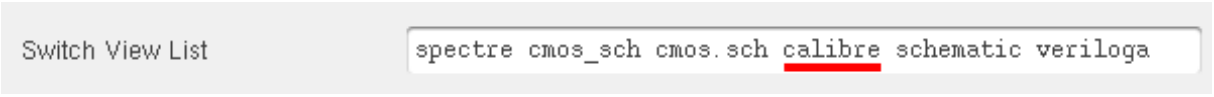


Figure 7.1: ADE environment settings

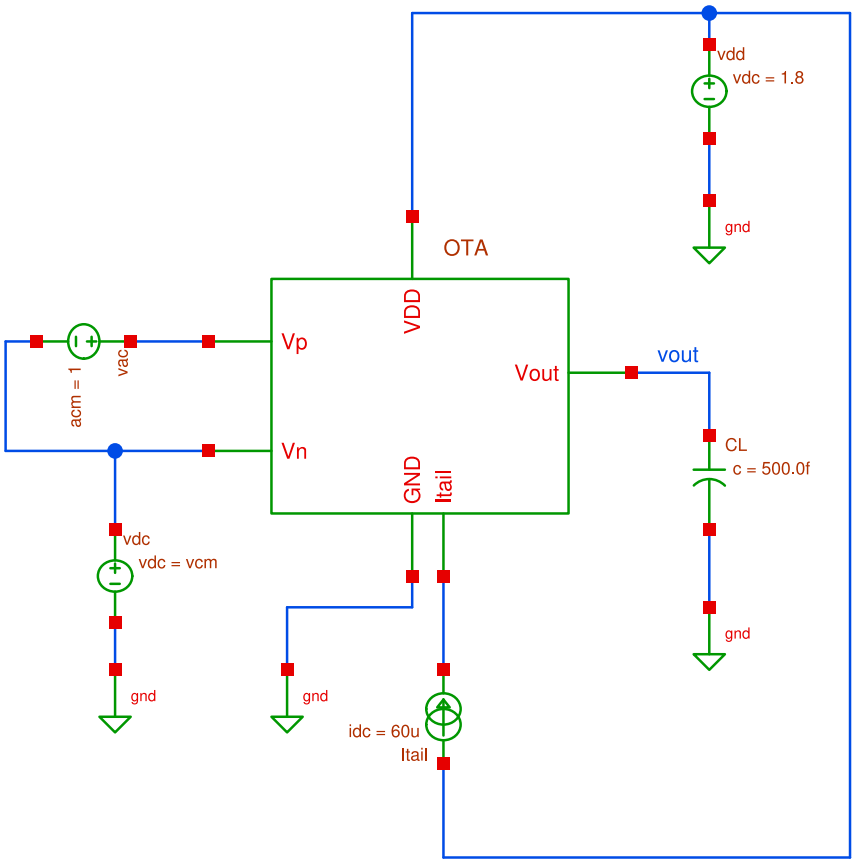
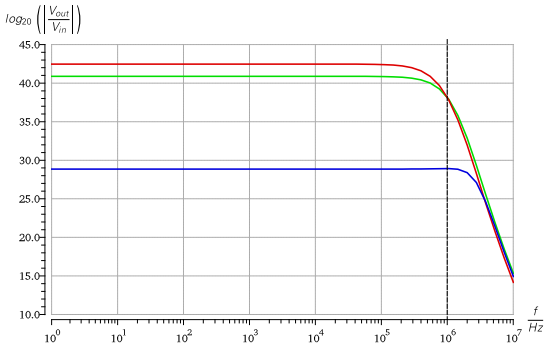
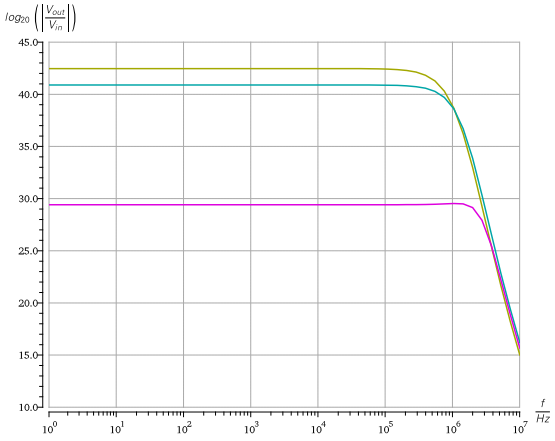


Figure 7.2: OTA testbench circuit

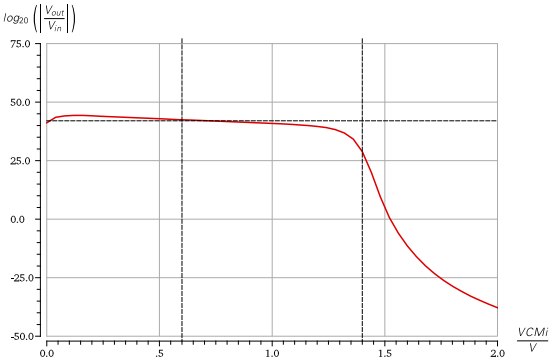
Below, the simulation results are shown side by side with those obtained from earlier schematic simulation.



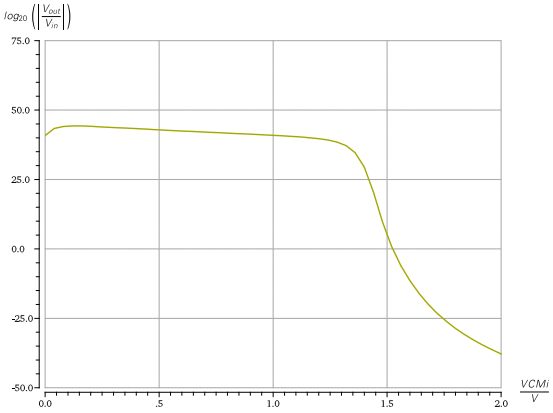
(a) Gain



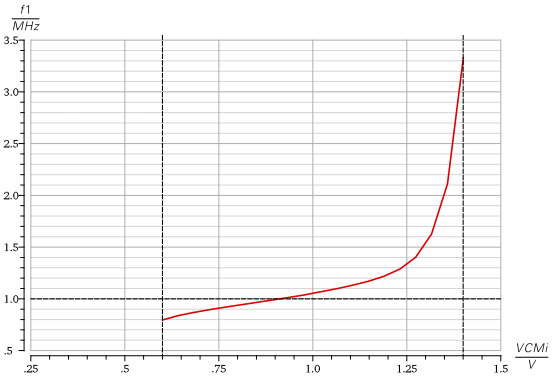
(b) Gain with parasitics



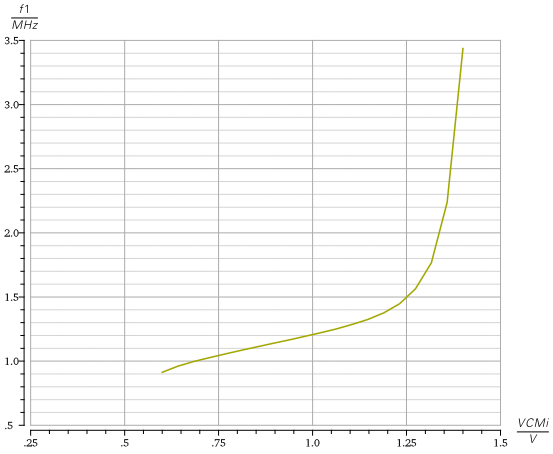
(c) DC gain



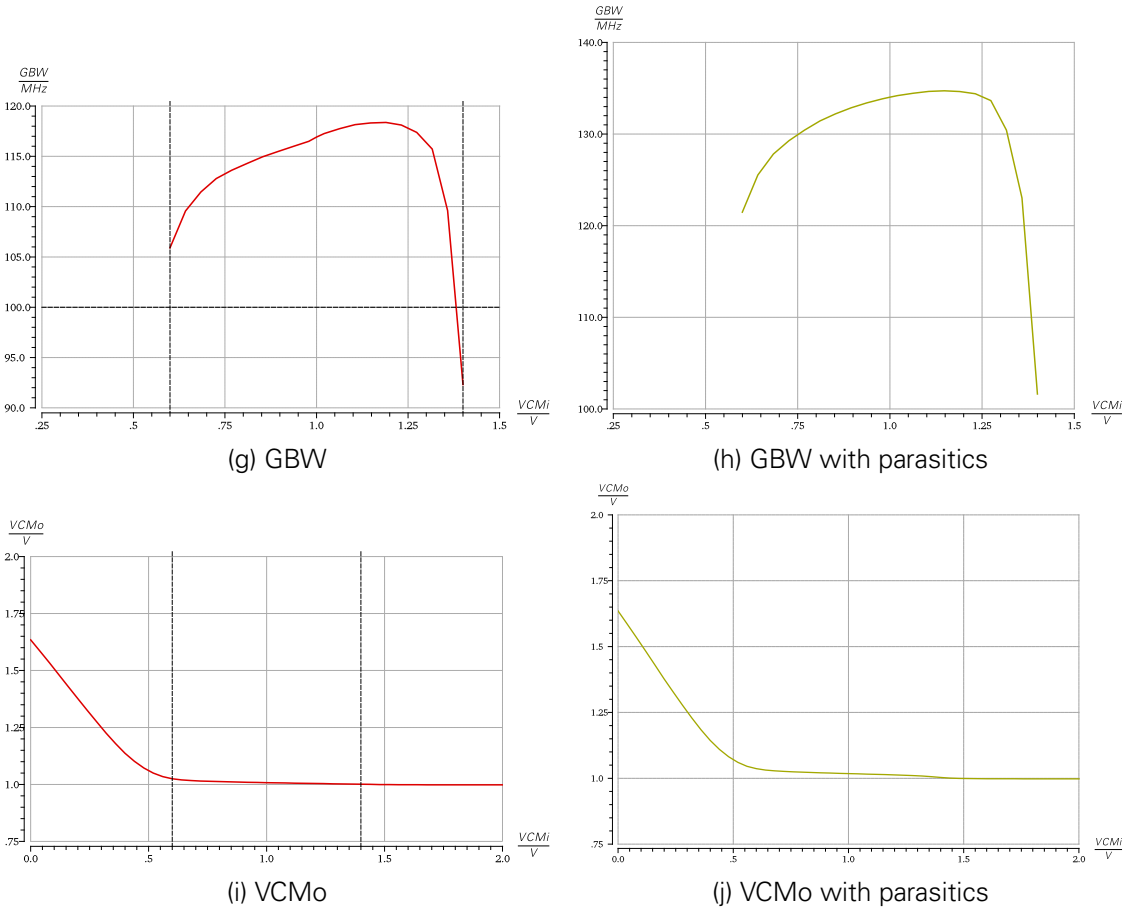
(d) DC gain with parasitics



(e) Bandwidth



(f) Bandwidth with parasitics



(g) GBW (h) GBW with parasitics

(i) VCMo (j) VCMo with parasitics

Figure 7.3: Comparison of schematic simulations with simulations with added parasitics

While for most parameters measured, the differences between simulation results obtained from the original schematic and those obtained for added parasitics are very small, in the latter case the bandwidth is noticeably larger over the whole input voltage range and for the gain bandwidth product this is even more pronounced. I was not able to determine whether this improved performance is a legitimate result of the added parasitics or stems from some error made during the design process.

8 CONCLUSION

Overall I had relatively few problems while designing this simple circuit. A large portion of the total time spent on this project was used up for the theoretical considerations which, while helping to improve my understanding of the circuit architecture, were ultimately not as useful as I thought they might be as was for example illustrated by the difference between the theoretical and practical sizing of the current mirror's transistors. Simulation was relatively straightforward, laying out the circuit was again time consuming and I initially struggled with a variety of design rule errors.

In conclusion I feel that I have gained a good grasp on the basic flow for designing integrated analog circuits especially when it comes to using *Virtuoso* and *Calibre*.